



REALTEK

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RTL8111H
RTL8111HS

**INTEGRATED 10/100/1000M ETHERNET
CONTROLLER FOR PCI EXPRESS APPLICATIONS**

LAYOUT GUIDE

(CONFIDENTIAL: Development Partners Only)

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REALTEK

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2014/01/10	First release.

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1. Introduction

The Realtek RTL8111H/RTL8111HS 10/100/1000M Ethernet controller combines a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8111H/RTL8111HS offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection and Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The RTL8111H/RTL8111HS supports the PCI Express 1.1 bus interface for host communications with power management, and complies with the IEEE 802.3u specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. It supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space. The RTL8111H/RTL8111HS features embedded One-Time-Programmable (OTP) memory. The RTL8111H/RTL8111HS provides a built-in switching regulator.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI MSI (Message Signaled Interrupt) and MSI-X are also supported.

In addition to the ACPI feature, remote wake-up (including AMD Magic Packet and Microsoft Wake-up frame) is supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e., main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8111H/RTL8111HS.

The RTL8111H/RTL8111HS is fully compliant with Microsoft NDIS5, NDIS6 (IPv4, IPv6, TCP, UDP) Checksum and Segmentation Task-offload (Large send and Giant send) features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The RTL8111H/RTL8111HS supports Receive Side Scaling (RSS) to hash incoming TCP connections and load-balance received data processing across multiple CPUs. RSS improves the number of transactions per second and number of connections per second, for increased network throughput.

The RTL8111H/RTL8111HS supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE). IEEE 802.3az operates with the IEEE 802.3 Media Access Control (MAC) Sublayer to support operation in Low Power Idle mode. When the Ethernet network is in low link utilization, EEE allows systems on both sides of the link to save power.

The device also features inter-connect PCI Express technology. PCI Express is a high-bandwidth, low-pin-count, serial, interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure.

The RTL8111H/RTL8111HS is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

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2. Design and Layout

System designers should follow basic rules in layout and placement, general termination, power supply filtering, plane partitioning, and EMI reduction in order to optimize designs that use the RTL8111H/RTL8111HS. Following these rules will greatly contribute to a properly functioning hardware system.

This guide has the following goals:

- (1) Create a low-noise, power-stable environment.
- (2) Reduce the degree of EMI/EMC and their influence on the RTL8111H/RTL8111HS.
- (3) Simplify the task of routing signal traces.

2.1. General Guidelines

In order to achieve maximum performance using the RTL8111H/RTL8111HS, good design practices are required throughout the process. The following are some recommendations for implementing a high-performance system.

- Provide a good power source to the RTL8111H/RTL8111HS. The power noise under normal operation must comply with the criteria in section 3.2.2, page 9. The voltage overshoot in the power-on procedure must comply with the criteria in section 7.1, page 21
- Verify that critical components such as the clock source and transformer meet application requirements
- Use bulk capacitors (4.7 μ F~10 μ F) between the power and ground planes
- Use 0.1 μ F de-coupling capacitors to reduce high-frequency noise on the power and ground planes
- Keep de-coupling capacitors close to the RTL8111H/RTL8111HS (within 200 mils)
- Provide termination on all high-speed switching signals
- Use a smaller package for the capacitor to reduce the package inductance

Use the following signal integrity techniques to reduce crosstalk:

- Shorter parallel routes
- Thinner dielectrics
- Proper termination
- Provide a solid ground plane

PCI Express TX/RX differential pairs should comply with the following requirements:

- Differential Return Loss $\geq 10\text{dB}$ (measured within a 50MHz~1.25GHz range)
- Common Mode Return Loss $\geq 6\text{dB}$ (measured within a 50MHz~1.25GHz range)
- Differential Impedance should be limited from 80 to 120ohms (100ohm recommended)
- Only PCB traces are allowed for signal routing (do not use flat/shielded cable)

2.2. *Differential Signal Layout Guidelines*

- Keep differential pairs as close as possible and route both traces as identically as possible, meaning width, length, and location
- Avoid vias and layer changes if possible
- Keep transmit and receive pairs away from each other. Run orthogonally, or separate via a ground plane if possible
- 0.1 μF common mode noise filter capacitors should be placed near the RTL8111H/RTL8111HS
- Ninety-degree trace angles should be avoided. We recommend that the traces turn at 45° angles as shown in Figure 1. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts

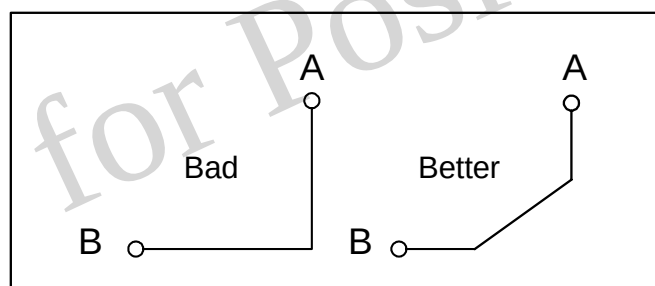


Figure 1. Signal Trace Angles

2.3. Placing the RTL8111H/RTL8111HS

- The RTL8111H/RTL8111HS should be placed as close as possible to the magnetics

2.4. Magnetics

- The magnetics should be placed at least 1500 mils away from the RJ-45 jack for surge protection (see section 11.1, page 33)
- The magnetics device, or devices with magnetic fields, should be separated and mounted at 90 degrees to each other

2.5. Crystal

- The Crystal should be placed away from I/O ports, important or high frequency signal traces (TX, RX, power), magnetics, and board edges
- The outer shield of the Crystal requires good grounding to avoid induction of EMC/EMI
- The retaining straps of the OSC, if any, need good grounding

2.6. Ferrite Beads and De-Coupling Capacitors

Each PCB design has its unique noise coupling behavior. Ferrite beads are used to suppress power noise. System designers are suggested to provide the option to replace the ferrite beads with 0Ω resistors. Decoupling capacitors should be placed as close as possible to the power pins, such that the distance from the IC power pin to the capacitor is less than 200 mils.

3. Power Noise Measurement

In order to achieve maximum performance when using the RTL8111H/RTL8111HS, a good power source of 3.3V with noise less than 200mV peak-to-peak, and 1.0V with noise less than 100mV peak-to-peak should be provided. The details of power noise measurement including measurement points, measurement criteria, and setting of scope are illustrated in the following sections.

3.1. Measurement Points

3.1.1. Measurement Points of 3.3V Power Noise on Schematics

In Figure 2, any de-coupling capacitor of VDDREG pins (CIN1, CIN2) and VDD33 pins (C1, C2) is available for 3.3V power noise measurement.

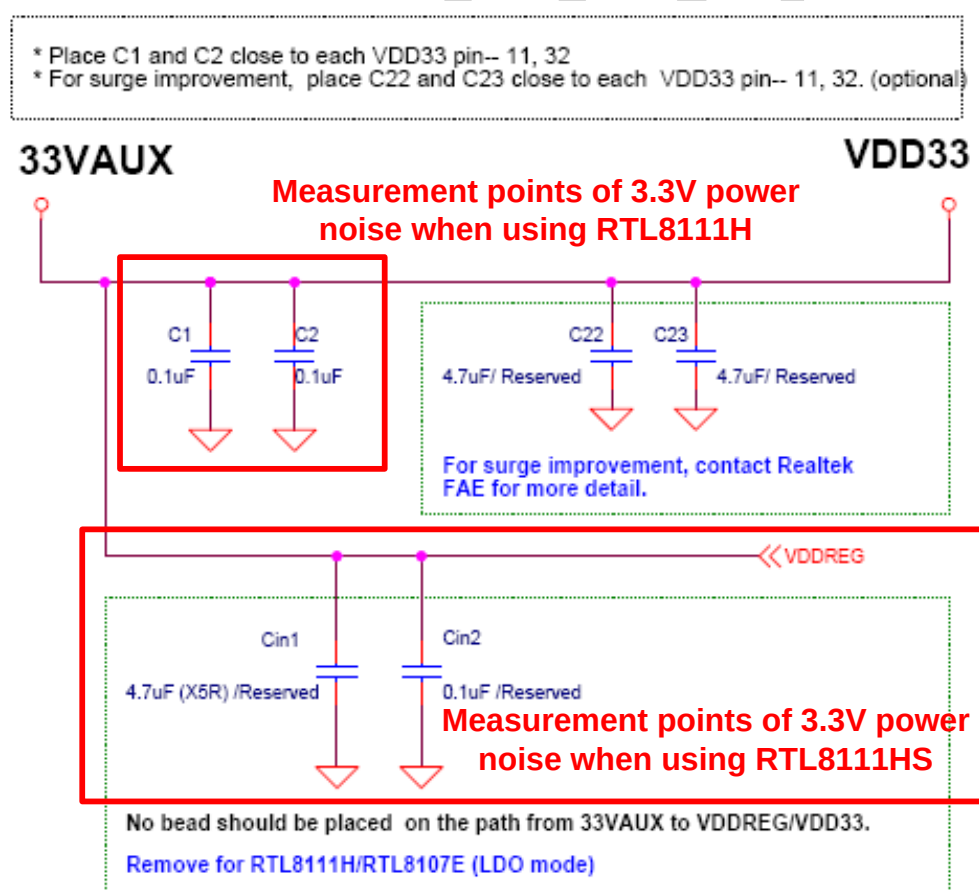


Figure 2. 3.3V Power Noise Measurement Point

3.1.2. Measurement Points of 1.0V Power Noise on Schematics

In Figure 3, any de-coupling capacitor of VDD10 pins (COUT1, COUT2, C3, C4, C5, C6, C7) is available for 1.0V power noise measurement.

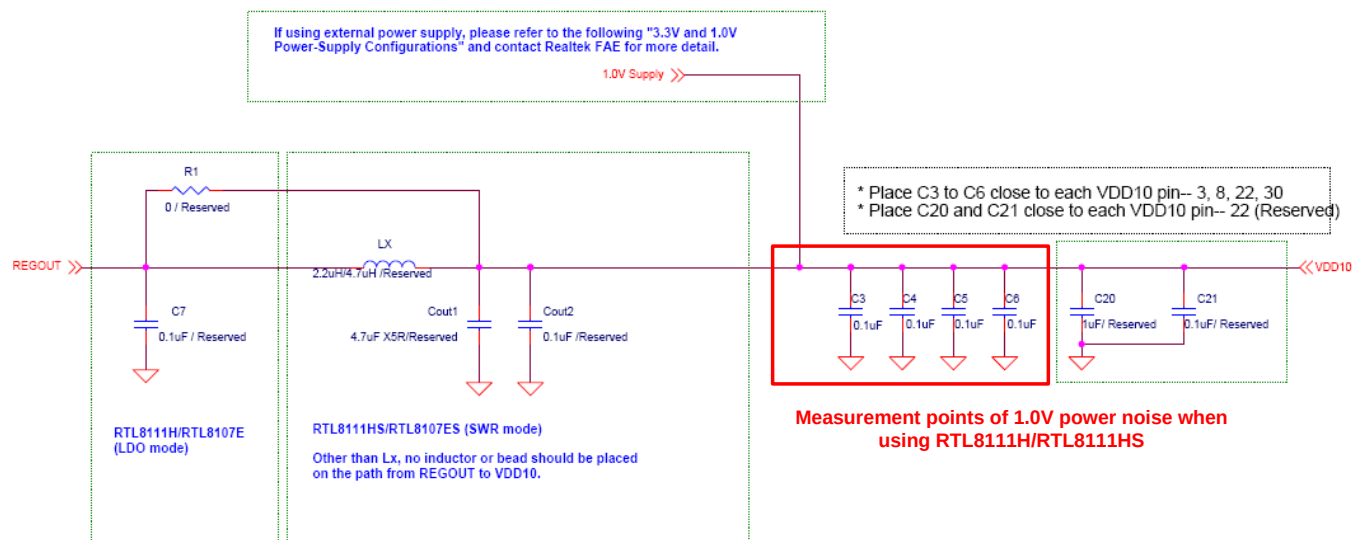


Figure 3. 1.0V Power Noise Measurement Point

3.2. Scenarios, Scope Setup, and Measurement Criteria

3.2.1. Scenarios and Scope Setup

Setup the scenarios:

- Choose one de-coupling capacitor as the measurement point of power noise, then solder a pair of solid conductors to both sides of the chosen capacitor
- Twist the solid-conductor pairs, and make them as short as possible
- Probe the single-end probe to the 3.3V/1.0V source, and GND to the twisted solid-conductor pairs on the capacitors
- System Status
 - System Power: ON
 - Transmit/Receive Data at 1Gbps mode
- Acquisition Mode: Sample
- Vertical Scale/Resolution: 50mV/div
- Horizontal Scale
 - Time Scale/Resolution: 2ms/div
 - Sampling Rate: 2.5 GHz, 400ps/pt
 - Number of Acquisitions: 2000acqs
- Measurement Bandwidth: 1GHz

These settings and illustrations are based on the following models of scope and probe.

- Tektronix: DPO 7104 (Digital Phosphor Oscilloscope), 1GHz
- Tektronix: P6245, $\geq 1.5\text{GHz}$

If a different model of scope or probe is used when doing the power noise measurement, ensure the scenario settings are as close as possible to those described above.

With the above scenarios and settings correctly done, the power noise measurement can be started.

3.2.2. Measurement Criteria

Criteria of voltage overshoot in the power-on procedure:

- A voltage overshoot may be observed in the power-on procedure and should be less than 4V (see section 7.1, page 21)

Power Noise Requirement under normal operation:

- 3.3V Power Noise < 200mV peak-to-peak (Figure 4)
- 1.0V Power Noise < 100mV peak-to-peak (Figure 5)

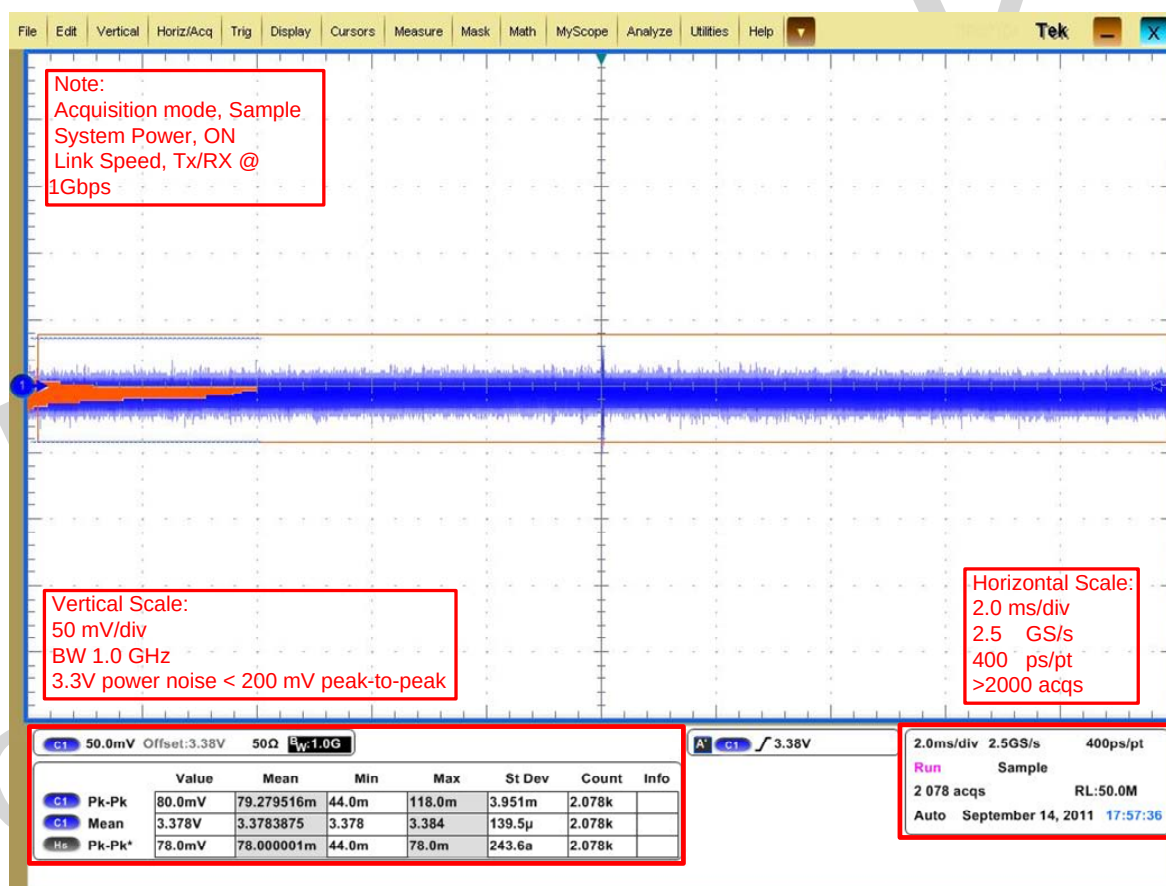


Figure 4. Measurement Criteria of 3.3V Power Noise

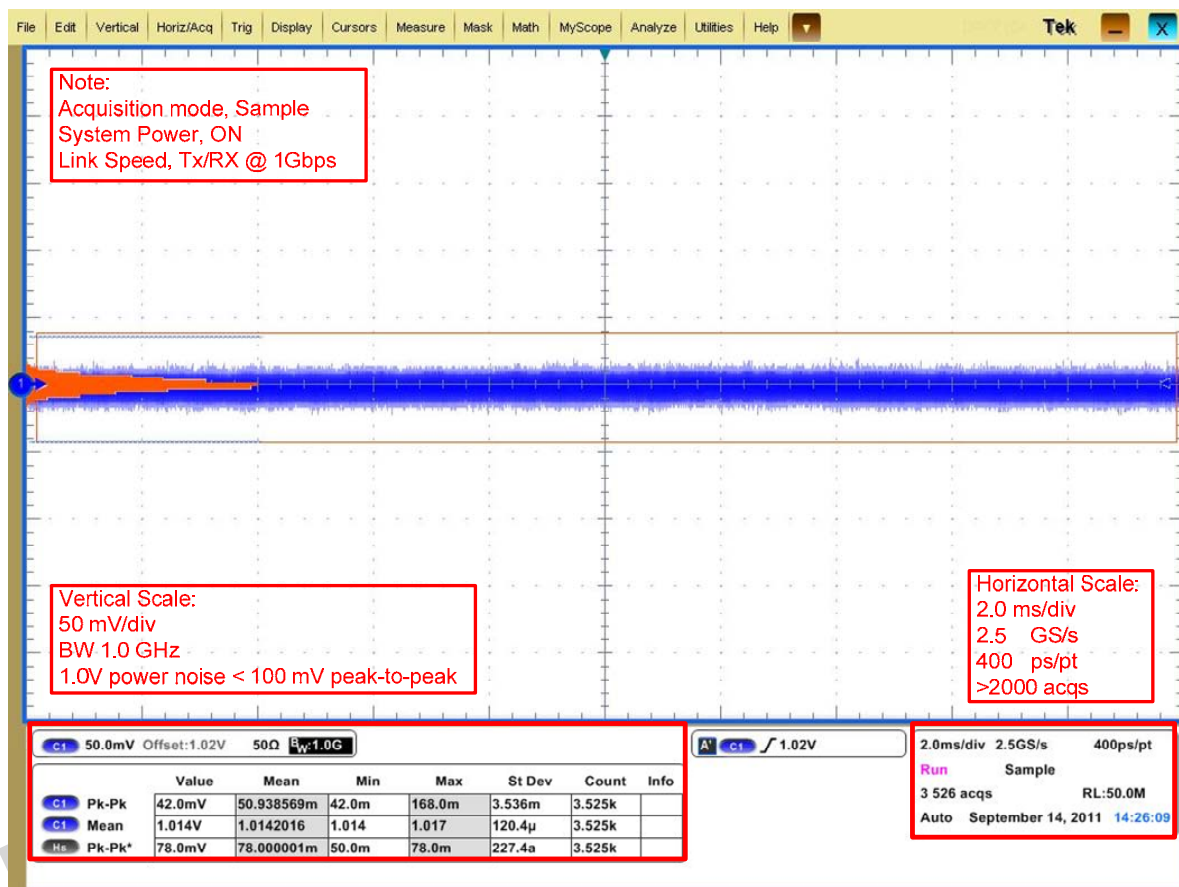


Figure 5. Measurement Criteria of 1.0V Power Noise

4. Signal and Trace Routing

Noise, ringing, and data lines should be controlled with proper termination. Power supply pins should be protected by proper filtering techniques. Good routing of traces can reduce propagation delay, crosstalk, and high frequency noise. It will also improve the signal quality to the receiver and reduce transmit signal losses.

- Traces routed from the RTL8111H/RTL8111HS to the 10/100/1000M magnetics, and to the RJ-45 connector, should be as short as possible. The 12cm maximum length between the RTL8111H/RTL8111HS and magnetics is achievable only when there is no interference. It is also very important to keep all four differential pair signal traces (MDI0+/-, MDI1+/-, MDI2+/-, MDI3+/-) equal in length. The two traces of each pair should be placed close to each other (D1) since they are differential pair signals to each other and provide a strong canceling effect on noise. The width of D1 should be calculated to have 100Ω impedance (Figure 6)

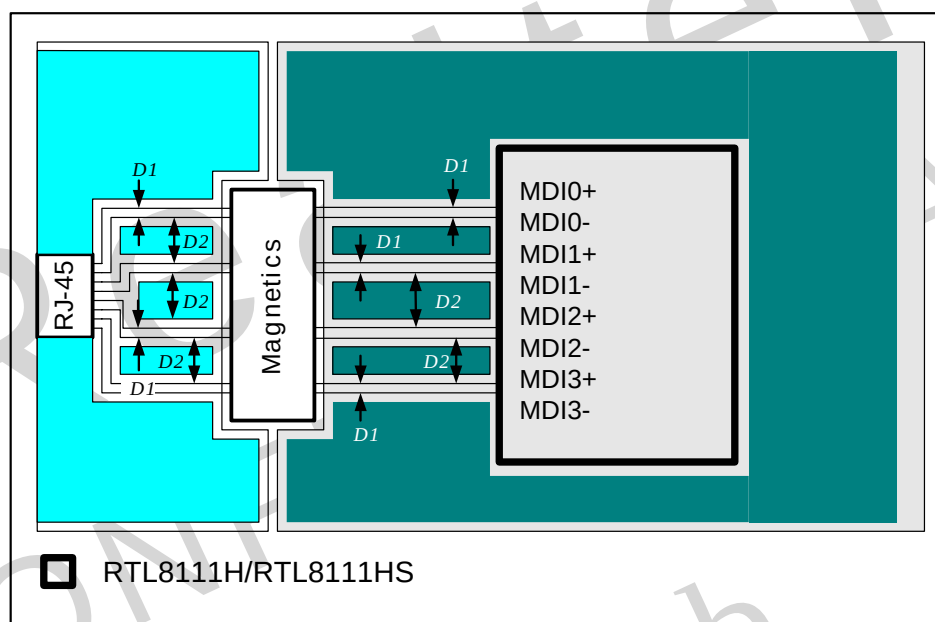


Figure 6. Signal & Trace Routing

- We suggest that there should be more than 30 mil spacing between different differential pairs to minimize crosstalk coupled from other pairs (D2 in Figure 6). In addition, Ground Plane shielding can be used to separate all four signal pairs. However, a good layout should avoid the following situations:
 - Intersection of any two pairs of signal traces
 - Intersection of the two signal traces of the same differential pair
- To minimize impedance mismatch, do not use vias on the four differential pairs (we recommend to place the four differential pairs on the same plane)

- Ninety-degree trace corners should be avoided. We recommend that the traces turn at 45° angles as shown in Figure 1, page 4. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts
- The trace length and the ratio of trace width to trace height above the ground planes should be carefully considered. If running power on the trace is unavoidable, the trace width should be wider than 60 mils, and properly filtered to minimize power noise effects. The clock and other high-speed signal traces should be as short and wide as possible (compared to normal digital traces). It is better to have a ground plane under these traces. If possible, use a ground plane to surround them
- It is important to separate Digital Signals (e.g., BOOTROM, Flash) from Analog Signals (e.g., MDI0+/-, MDI1+/-, MDI2+/-, and MDI3+/-, RSET) in order to avoid interference. If it is unavoidable to cross digital signals with analog power, do it at 90° angles
- The power into the RTL8111H/RTL8111HS digital power pins can be improved with de-coupling capacitors. The Power signal traces (de-coupling cap traces, power traces, grounding traces) should be as short and wide as possible. The vias of the de-coupling capacitor should be large enough in diameter. All analog power pins on the RTL8111H/RTL8111HS need to be de-coupled with a capacitor. The de-coupling capacitors should be placed as close to the IC as possible and the traces should be kept short
- The PCI Express signal differential pairs should be 5 mils wide, with a spacing of 7 mils between them (REFCLK+ & REFCLK-, HSOP & HSON, HSIP & HSIN). The length difference of the signals in a pair should not exceed 5 mils. For example, if HSON is 900 mils and HSOP is 890 mils, it may result in data transmit error

5. Ground and Power Plane Layout

5.1. Ground Plane Layout

There is only one ground plane for analog power (AVDD33, AVDD10) and digital power (DVDD33, DVDD10). In the center of the IC, there is an Exposed Pad (EPAD) ground. The size of the center EPAD ground is 2.7mm x 2.7mm. The PCB layout requires at least 4 vias to connect the EPAD to the lower layer ground plane (see Figure 7).

Isolated separation between Analog and Digital Ground domains is not recommended since bad ground plane partitioning could cause serious EMI emissions and degrade analog performance due to bouncing noise.

Whether there is sufficient space on the PCB for an isolated separation layout must also be taken into consideration. The key point of such a layout is to keep the analog GND return path approximately equal to the common GND. If the system designer is not comfortable doing this, just place a single ground plane with no partition.

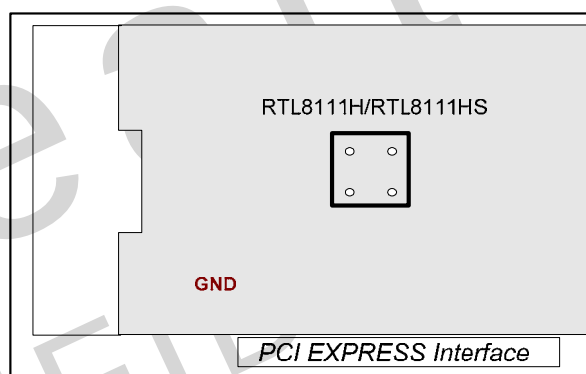


Figure 7. Ground Plane Layout-1

To achieve better ground plane performance, we recommend keeping the plane as large and uniform as possible. Figure 8 illustrates a not so good (left) and a good ground plane layout (right).

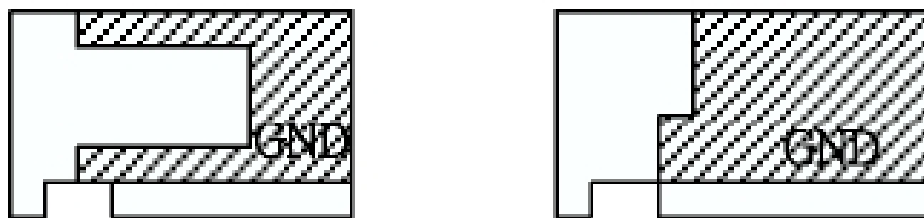


Figure 8. Ground Plane Layout-2

The plane area beneath the magnetics should be left void. The void area is to keep transformer-induced noise away from the power and system ground planes (Figure 9).

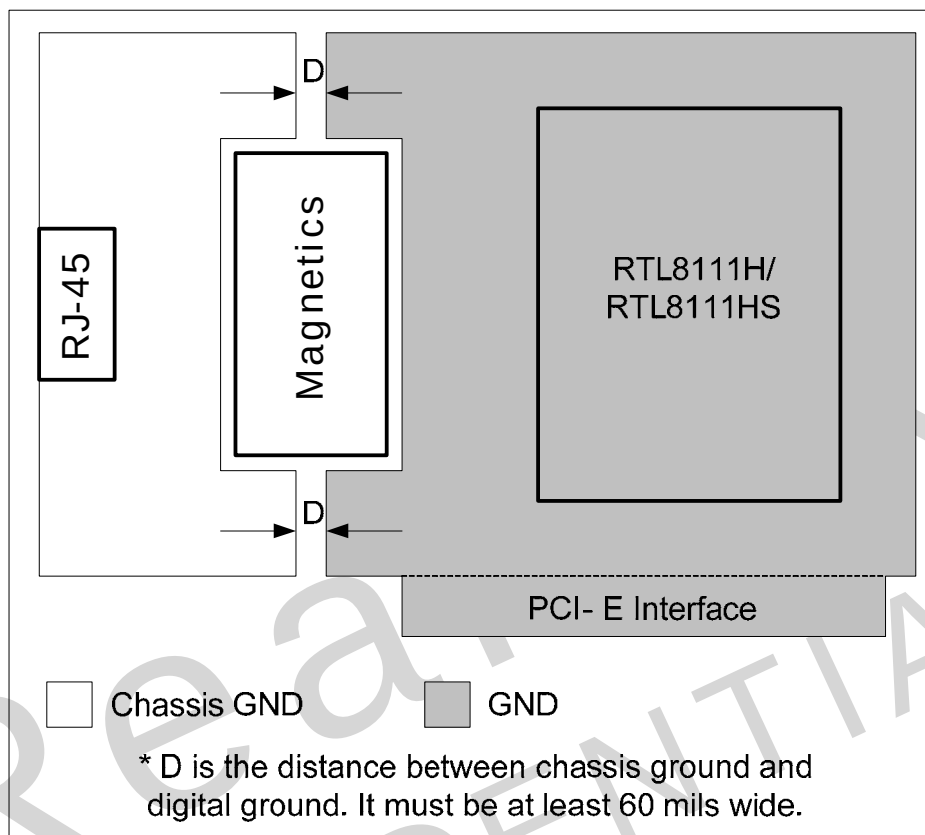


Figure 9. Ground Plane Separation

The Chassis Ground as shown in Figure 9 is known as an 'Isolated Ground'. It connects directly to the RJ-45 connector (fully shielded is recommended). In addition, a 2kV (3kV recommended) high voltage capability capacitor is needed to connect to this chassis ground for ESD protection.

It is also important to keep the gap (D in Figure 9) between Chassis GND and System GND wider than 60 mils for better isolation.

5.2. Power Plane Layout

The digital power plane should be separated from analog areas, which are extremely sensitive to noise. We recommend using at least a 4-layer PCB.

A low-pass filter combination of a ferrite bead and capacitors should be used to provide a clean, filtered power plane for analog consideration. It is important to avoid using unnecessary power traces to the RTL8111H/RTL8111HS, however, if it is unavoidable, try to keep these traces as short and wide as possible and make good use of vias.

(a) Decoupled Capacitor Example

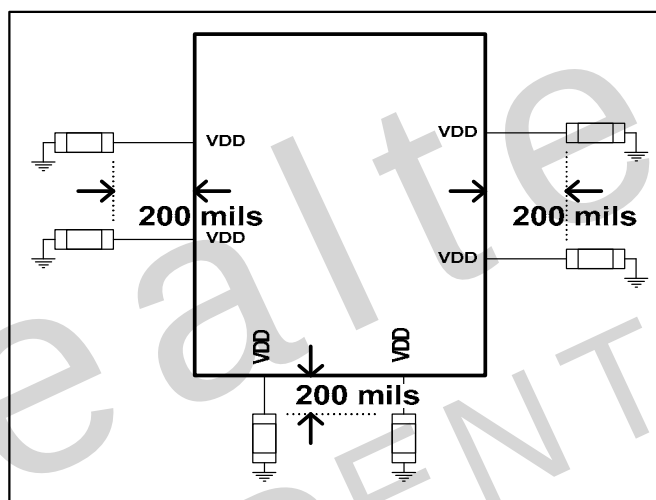


Figure 10. Decoupled Capacitor Example

(b) Use a Ferrite Bead or 0 ohm Resistor to Connect Digital and Analog Power

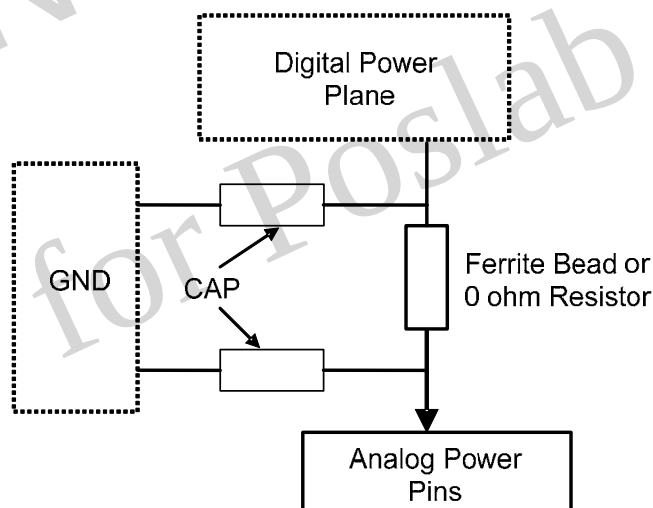


Figure 11. Power Plane

To further improve the performance of the power plane, try to keep the contact area between the RTL8111H/RTL8111HS VDD pins and power plane as large as possible rather than using small narrow traces (Figure 12).

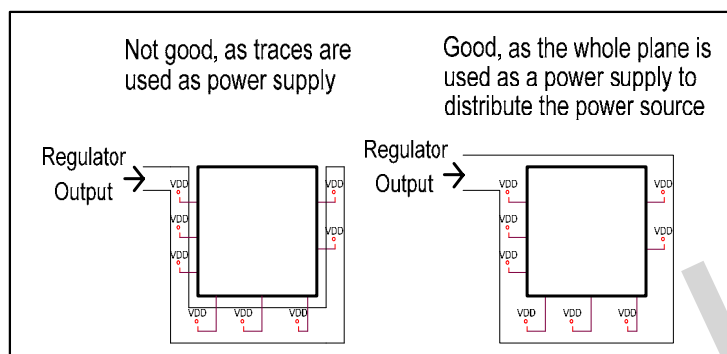


Figure 12. Power Source Distribution

- Keep power noise levels below 200mV peak-to-peak of 3.3V power, and 100mV peak-to-peak of 1.0V power in gigabit mode (refer to section 3.2.2, page 9 for details)
- All 3.3V/1.0V decoupling capacitors shown in the reference schematic should be used in all designs
- Keep the analog power (1.0V) plane as whole and as large as possible

5.3. Four-Layer Board Plane Layout

1. Signal 1 (top layer)
2. GND
3. Power
4. Signal 2 (bottom)

5.3.1. Signal 1 Plane Layout (Top Layer)

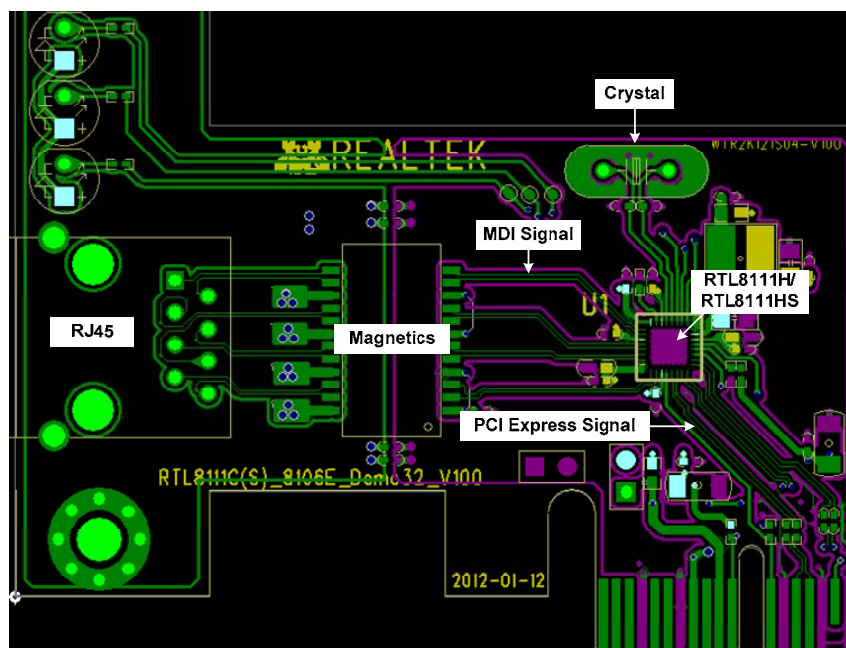


Figure 13. Signal 1 Plane Layout (Top Layer)

5.3.2. Ground Plane Layout (Layer 2)

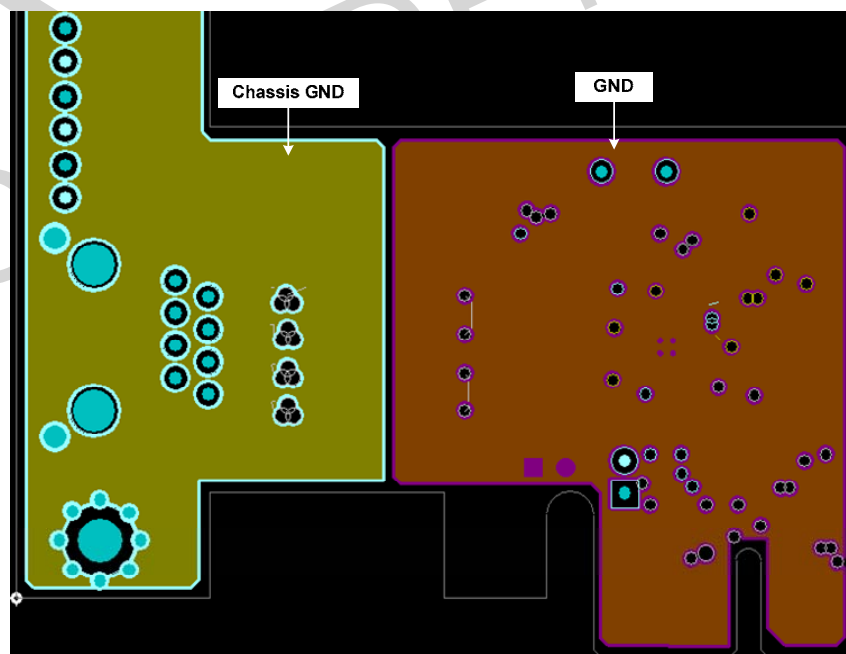


Figure 14. Ground Plane Layout (Layer 2)

5.3.3. Power Plane Layout (Layer 3)

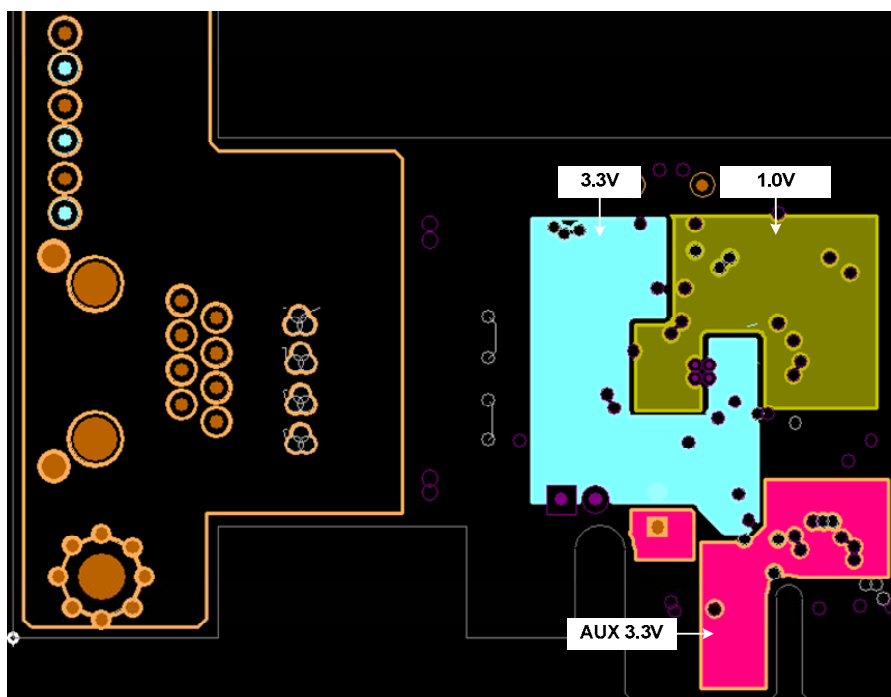


Figure 15. Power Plane Layout (Layer 3)

5.3.4. Signal 2 Plane Layout (Bottom Layer)

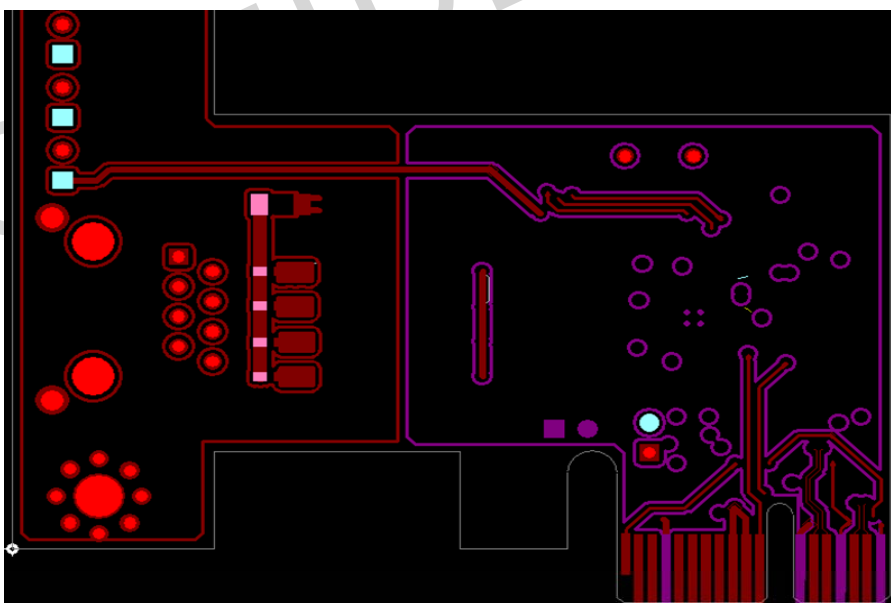


Figure 16. Signal 2 Plane Layout (Bottom Layer)

6. Center-Tapping

- A center-tapped fine-tuned capacitor (C1 Value: $0.01\mu\text{F}\sim 0.4\mu\text{F}$) can improve EMI for single tone noise. The capacitor default is $0.01\mu\text{F}$
- Changing the R2 resistor to a capacitor (Value: $0.01\mu\text{F}\sim 0.4\mu\text{F}$), and fine-tuning the connection to GND can improve EMI for single tone noise. The resistor default is 0 ohm

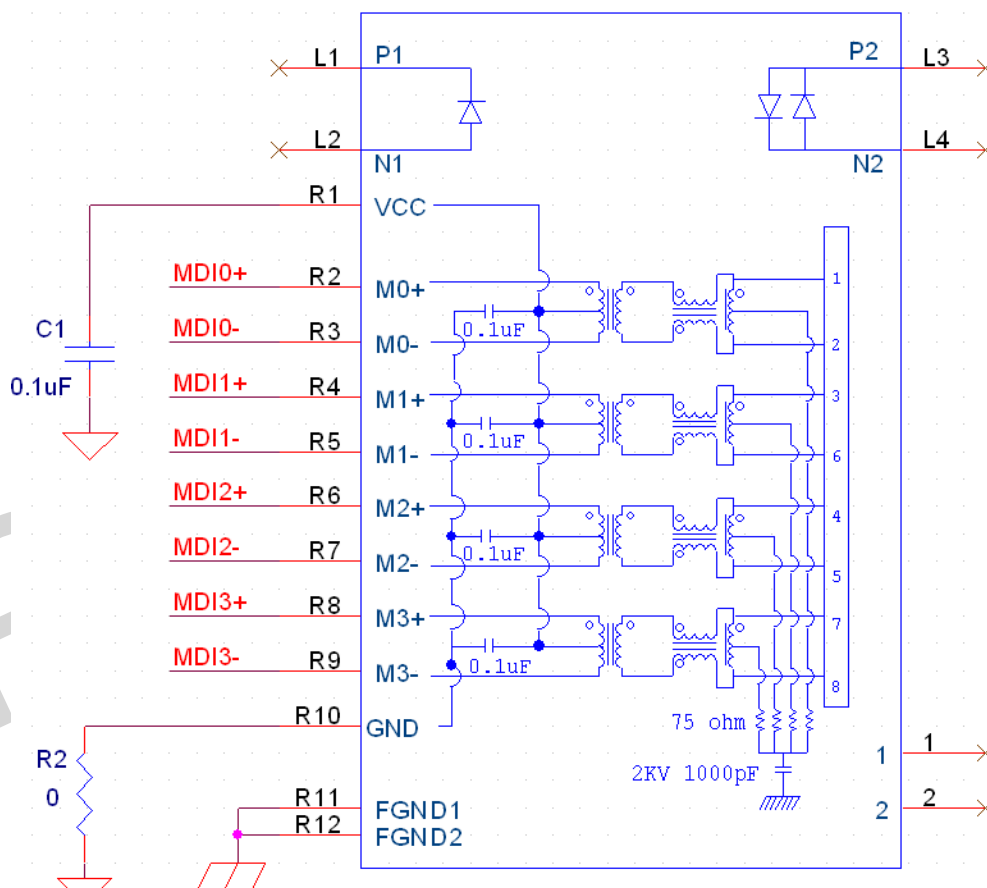


Figure 17. Center-Tapping

- When using a separate transformer, the center-tap MUST be aggregated (pins 10, 7, 4, 1) (C8 Value: 0.01 μ F~0.4 μ F) (see Figure 18)

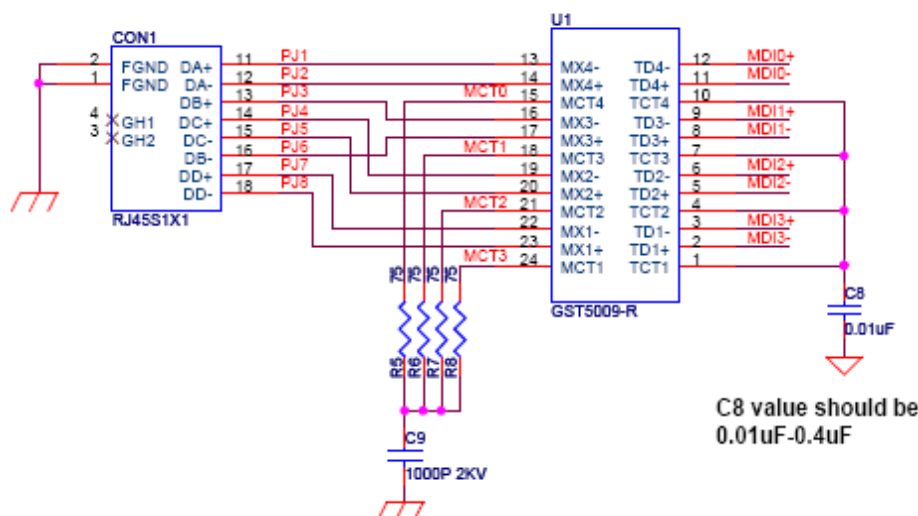


Figure 18. Separate Transformer

7. Switching Regulator (RTL8111HS only)

The RTL8111HS incorporates a state-of-the-art switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot. Note that the switching regulator 1.0V output pin (REGOUT) must be connected only to DVDD10 and AVDD10 (do not provide this power source to other devices).

7.1. Measurement Criteria

In order for the switching regulator to operate properly, the input and output voltage measurement criteria must be met. From the input side, the voltage overshoot cannot exceed 4V; otherwise the chip may be damaged. Note that the voltage signal must be measured directly at the VDDREG pin, not at the capacitor. In order to reduce the input voltage overshoot, the Cin1 and Cin2 must be placed close to the VDDREG pin. The following figures show what a good input voltage and a bad one look like.

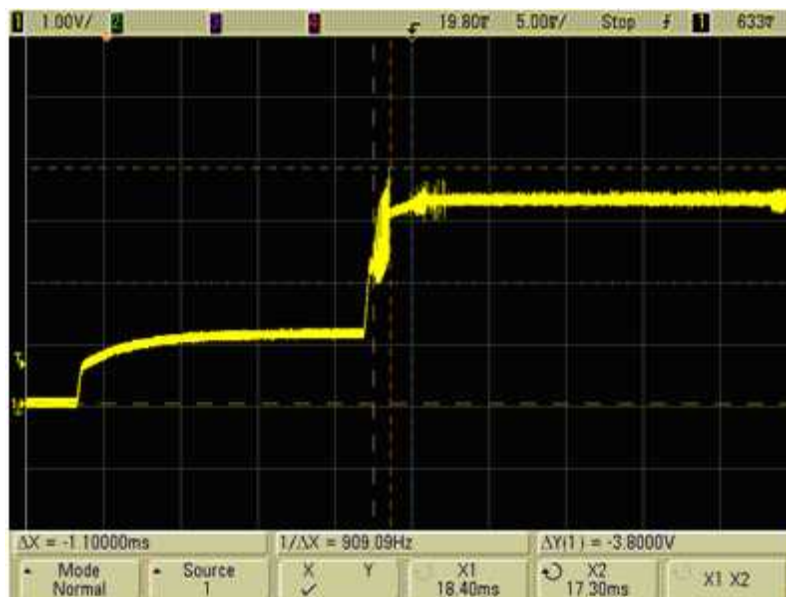


Figure 19. Input Voltage Overshoot <4V (Good)

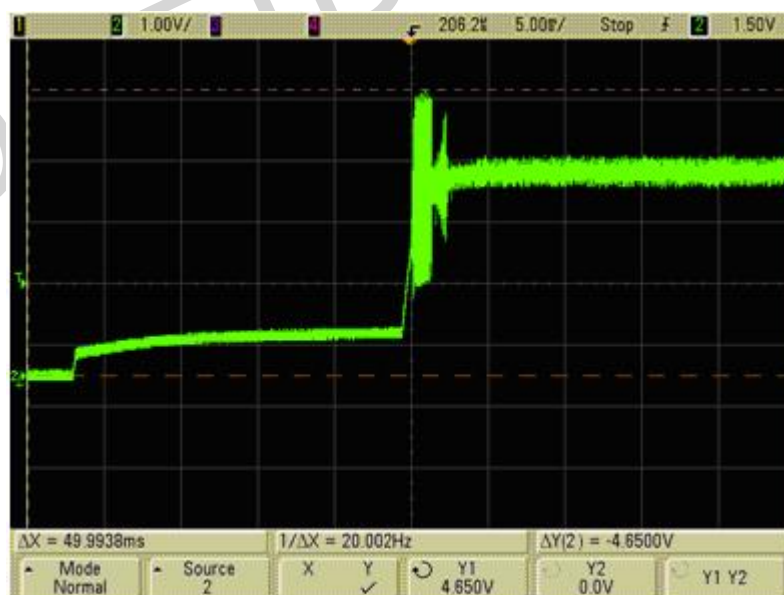


Figure 20. Input Voltage Overshoot >4V (Bad)

From the output side measured at the REGOUT pin, the voltage ripple must be within 100mV peak-to-peak. Choosing different types and values of input and output capacitor (Cin1, Cin2; Cout1, Cout2) and power inductor (Lx) will seriously affect the efficiency and output voltage ripple of switching regulators. The following figures show the effects of different types of capacitors on the switching regulator's output voltage.

The blue square wave signal (top row) is measured at the output of the REGOUT pin before the power inductor (Lx). The yellow signal (second row) is measured after the power inductor (Lx), and shows there is a voltage ripple. The green signal (lower row) is the current. Data in the following figures was measured at gigabit speed.



Figure 21. Ceramic 10μF 0603 X5R (Good)



Figure 22. Ceramic 4.7μF 0805 X5R (Ripple 12.4mV)

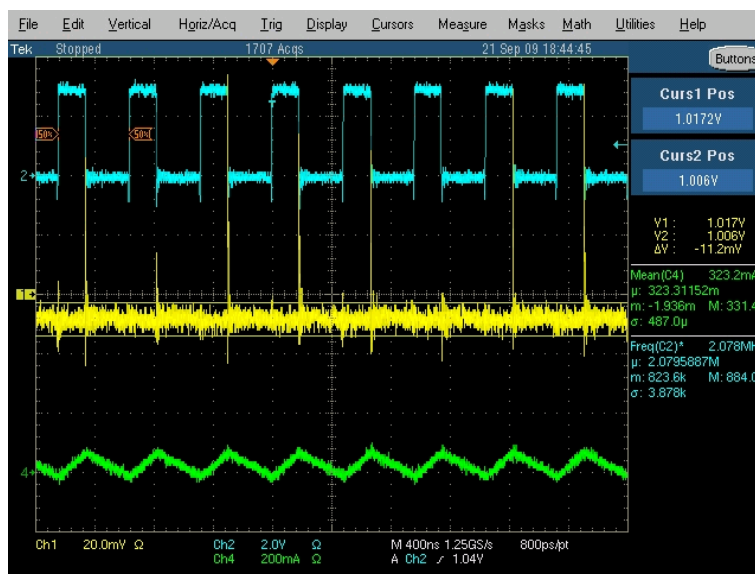


Figure 23. Ceramic 10 μ F 0603 X5R (Ripple 11.2mV)

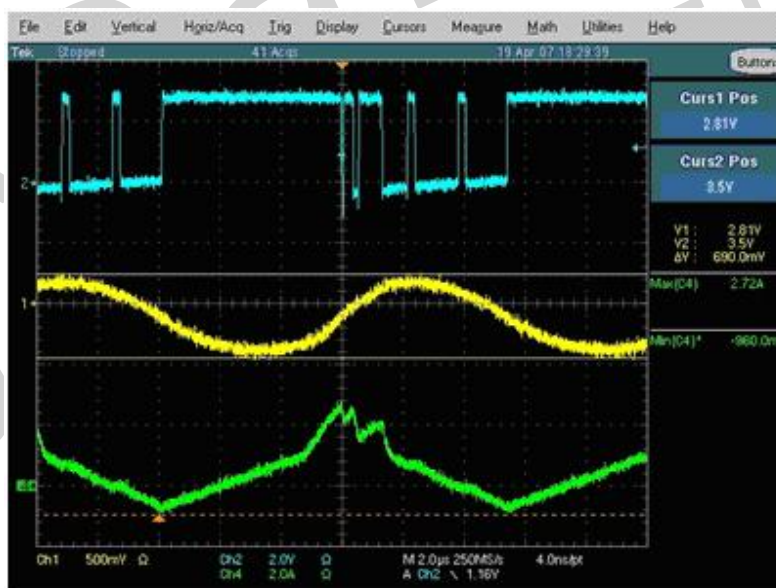


Figure 24. Ceramic 10 μ F (Y5V) (Bad)

A ceramic 10 μ F (X5R) will have a lower voltage ripple compared to an electrolytic 100 μ F. The key to choosing a proper output capacitor is to choose the lowest ESR to reduce the output voltage ripple. Choosing a ceramic 10 μ F (Y5V) in this case will cause malfunction of the switching regulator. Placing several Electrolytic capacitors in parallel will help lower the output voltage ripple.



Figure 25. Electrolytic 100μF (Ripple Too High)

The following figures show how different inductors affect the REGOUT pin output waveform. The typical waveform should look like Figure 26, which has a square wave with a dip at the falling edge and the rising edge. If the inductor is not carefully chosen, the waveform may look like Figure 27, where the waveform looks like a distorted square wave. This will cause insufficient current supply and will undermine the stability of the system at gigabit speed. Data in the following figures was measured at gigabit speed.

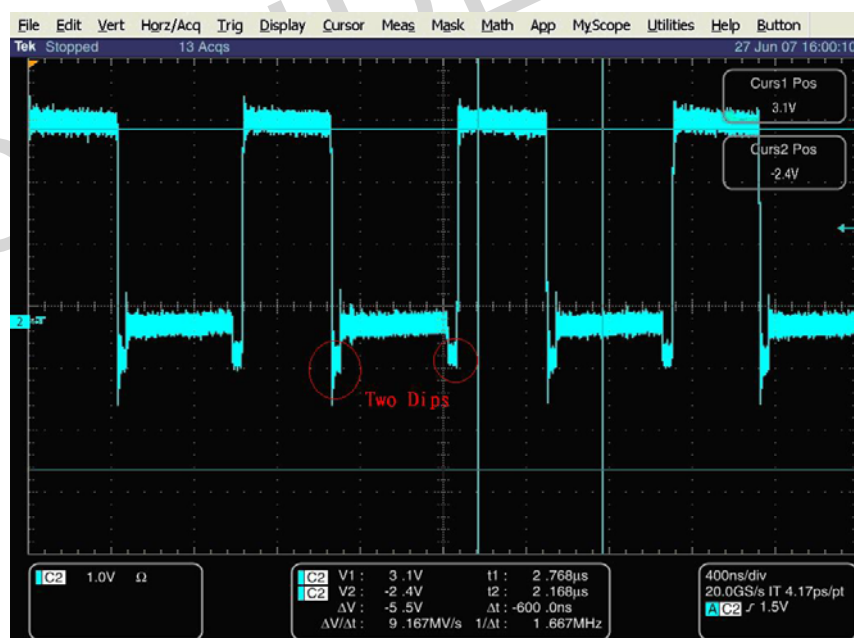


Figure 26. 2.2μH Inductor (Good)

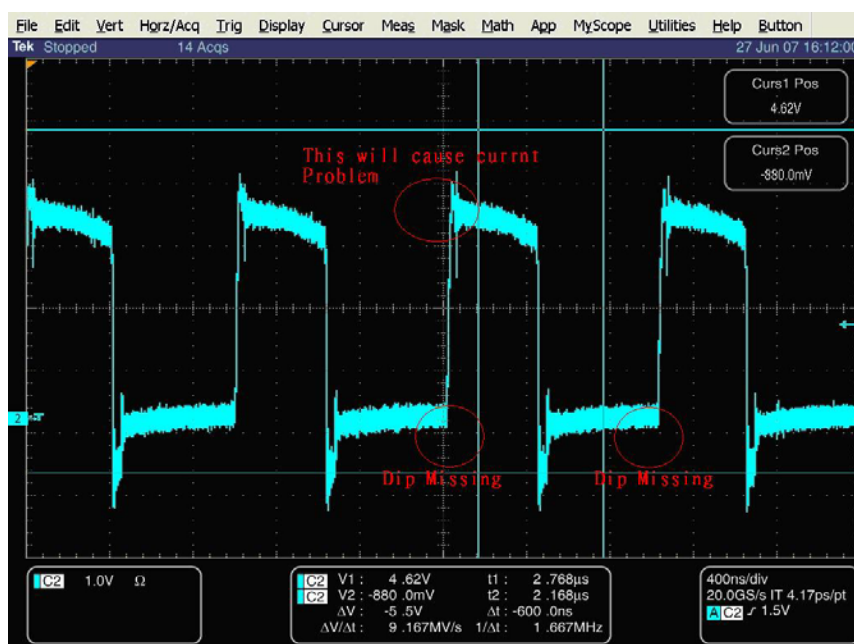


Figure 27. 1µH Bead (Bad)

7.2. Efficiency Measurement

The efficiency of the switching regulator is designed to be above 75% in gigabit traffic mode. It is very important to choose a suitable inductor before Gerber certification, as the Inductor ESR value will affect the efficiency of the switching regulator. An inductor with a lower ESR value will result in a higher-efficiency switching regulator.

The efficiency of the switching regulator is easily measured using the following method.

Figure 28, page 26, shows two checkpoints, checkpoint A (CP_A) and checkpoint B (CP_B). The switching regulator input current (Icpa) should be measured at CP_A, and the switching regulator output current (Icpb) should be measured at CP_B.

To determine efficiency, apply the following formula:

$$\text{Efficiency} = V_{cpb} \cdot I_{cpb} / V_{cpa} \cdot I_{cpa}$$

Where V_{cpb} is 1.0V; V_{cpa} is 3.3V. The measurements should be performed in gigabit traffic mode.

For example:

- The ESR value @ 1MHz is approximately 0.712ohm
- The measured Icpa is 72mA at CP_A

- The measured I_{cpb} is 203mA at CP_B

These values are measured in gigabit traffic mode, so the efficiency of the GOTREND GTSD32-4R7M can be calculated as follows:

$$\text{Efficiency} = (1.0V \times 203mA) / (3.3V \times 72mA) = 0.854 = 85.4\%.$$

We recommend that when choosing an inductor for the switching regulator, the efficiency should be measured, and that the inductor should yield an efficiency rating higher than 75%. If the efficiency does not meet this requirement, there may be risk to the switching regulator reliability over the long term.

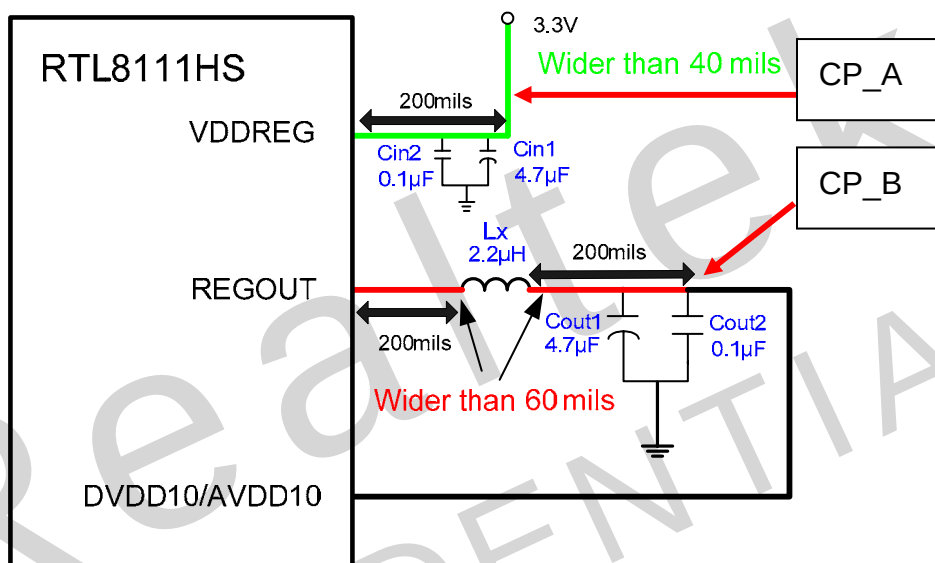


Figure 28. Switching Regulator Efficiency Measurement Check Point

8. Recommendations for Buck Circuit PCB Layout

8.1. LDO (RTL8111H)

- The input 3.3V power trace connected to VDDREG must be wider than 40 mils
- The output power trace out of REGOUT must be wider than 60 mils
- C7 (0.1 μ H) must be kept within 200 mils (0.5 cm) of REGOUT
- Do not use vias on VDDREG and REGOUT traces

Note: Violation of the above rules will damage the IC.

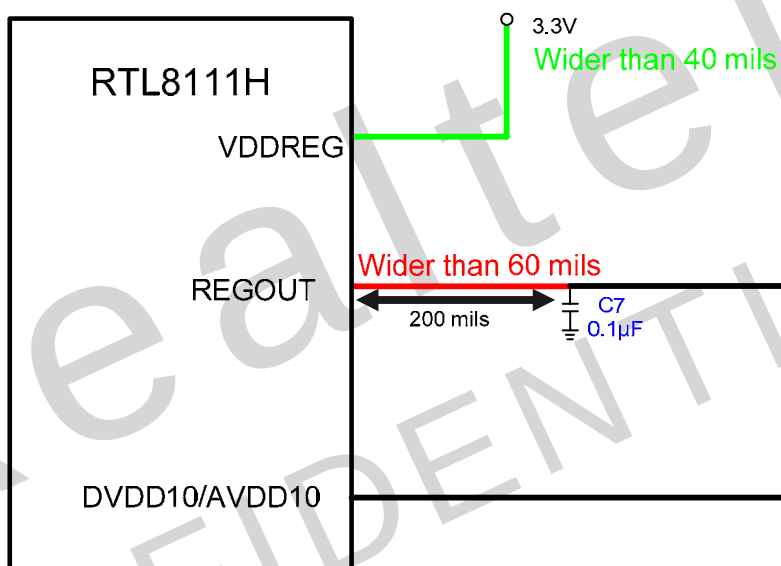


Figure 29. LDO Related Layout Recommendations

8.2. Switching Regulator (RTL8111HS)

- The input 3.3V power trace connected to VDDREG must be wider than 40 mils
- The bulk de-coupling capacitors (Cin1 and Cin2) must be placed within 200 mils (0.5 cm) of VDDREG to prevent input voltage overshoot
- The output power trace out of REGOUT must be wider than 60 mils
- Lx (2.2 μ H) must be kept within 200 mils (0.5 cm) of REGOUT
- Cout1 and Cout2 must be kept within 200 mils (0.5 cm) of Lx to ensure stable output power and better power efficiency
- For switching regulator stability, the capacitor Cout1 and Cout2 must be a ceramic (X5R) capacitor. Cin1 and Cin2 are recommended to be ceramic capacitors
- Place Lx and Cin1 on the same layer as the RTL8111HS. Do not use vias on VDDREG and REGOUT traces
- Other than Lx (2.2 μ H), no inductance or bead should be placed on the path from REGOUT to DVDD10/AVDD10

Note: Violation of the above rules will damage the IC.

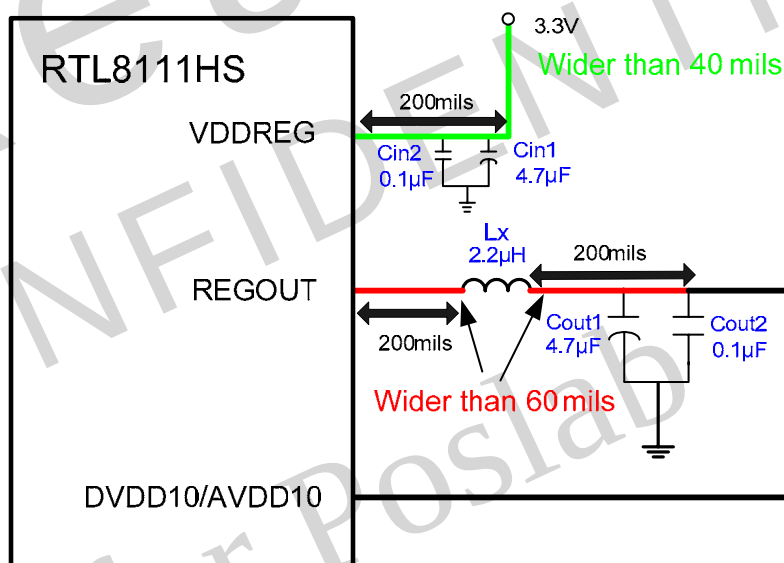


Figure 30. SWR Related Layout Recommendations

9. Power Sequence Specifications

9.1. Power Sequence

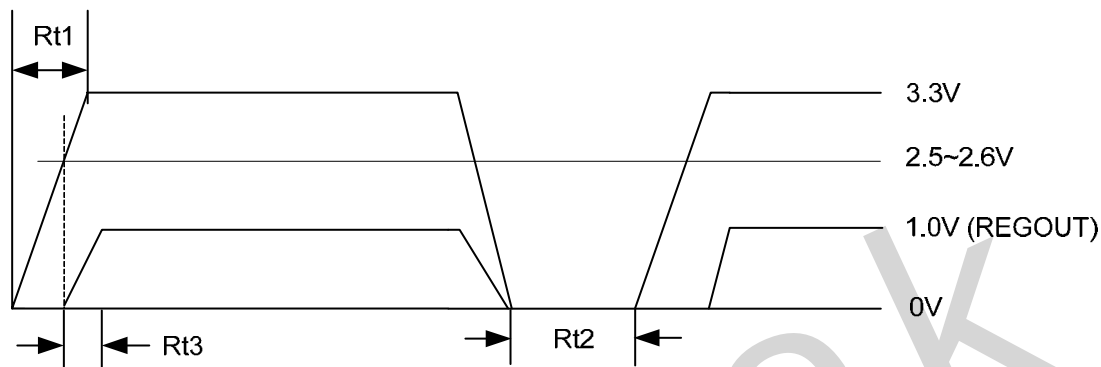


Figure 31. Power Sequence

Table 1. Power Sequence Parameters

Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	0.5	-	100	ms
Rt2	3.3V Off Time	50	-	-	ms
Rt3	1.0V (REGOUT) Settle Time	-	-	15	ms

Note: See the following section for power sequence requirements.

9.2. Power Sequence Parameters

Rise Time > 0.5ms

No action to take.

Rise Time 0.1ms~0.5ms

If the rise time is between 0.1ms and 0.5ms, the customer MUST ensure that there is at least three times as much margin for inrush current to the RTL8111H/RTL8111HS so as to be safely under the system's 3.3V OCP threshold.

For example:

- Assume customer supply power rise time of the RTL8111H/RTL8111HS is 0.374ms
- The system 3.3V OCP is 9A
- The inrush current of other 3.3V devices is 5.64A

The inrush current to the RTL8111H/RTL8111HS must be less than 1.12A, otherwise an unanticipated system OCP may be triggered. It can be expressed in the following formula:

Inrush current to the RTL8111H/RTL8111HS < (System 3.3V OCP - inrush current of other 3.3V devices) / 3

Rise Time < 0.1ms

If the rise time is less than 0.1ms, there is risk of an unanticipated ESD trigger event, which may cause permanent damage to the RTL8111H/RTL8111HS.

If there is any action that involves consecutive ON/OFF toggling of the switching-regulator source (3.3V), the design must make sure the OFF state of both the switching-regulator source (3.3V) and output (1.0V) reach 0V, and the time period between the consecutive ON/OFF toggling action must be longer than 50ms.

10. Parts Recommendations

10.1. 10/100/1000M Magnetic

Turn Ratio TX/RX: 1:1

Primary Inductance: 350 μ H OCL with 8mA bias

Insertion Loss: -1.0dB Max, 1 ~ 100MHz

Return Loss: -18dB Min @ 100 Ω , 1 ~ 30MHz
 -14dB Min @ 100 Ω , 30 ~ 60MHz
 -12dB Min @ 100 Ω , 60 ~ 80MHz

Differential to Common Mode Rejection:

-40dB Min @ 1 ~ 60MHz
 -30dB Min @ 60 ~ 100MHz

Hi-Pot: 1500Vrms @ 60sec

Operating Temperature: 0°C to 70°C

Recommended Magnetics: Pulse H5007 or similar

10.2. Reference Clock

A 25MHz/48MHz (within 50ppm) parallel resonant crystal can be used as the reference clock source to replace the 25MHz/48MHz Oscillator. The crystal must be connected to CKXTAL1 (Pin 28) and CKXTAL2 (Pin 29). Shunt each crystal lead to ground with a 27pF capacitor.

Parameters	Range
Frequency	25MHz/48MHz
Temperature Stability	± 10 ppm
Duty Cycle	50% ± 10 %
Tolerance	± 50 ppm
ESR	Max 30 Ω
Broadband Peak-to-Peak Jitter*	Max 200ps
Aging	5ppm/year, max.

Note: Broadband RMS=9ps; 25KHz to 25MHz RMS=3ps.

10.3. Resistors

Resistors that have tolerance requirements within 1% are recommended. Refer to the provided BOM for suggested schematics.

10.4. Capacitors

For switching regulator power filtering, use X5R Ceramic capacitors for the power circuit.

10.5. Ferrite Bead

The ferrite bead used should be of at least $100\Omega@100\text{MHz}$ impedance with a rated current of 300mA or higher.

10.6. Power Inductor

The power inductor used by the switching regulator should be able to withstand 600mA of current. The variance in the inductance value should be less than 20% under 600mA of current. The resistance value should be as small as possible to achieve the expected switching regulator efficiency, which must be higher than 75%.

Typically, if the power inductor's ESR at 1MHz is below 0.8Ω , the switching regulator efficiency will be above 75%. However, the actual switching regulator efficiency must be measured according to the method described in section 7.2 Efficiency Measurement, page 25.

10.7. RJ-45 Jack

A fully shielded RJ-45 connector should be used.

11. Surge Protection

In order to provide adequate surge protection for the RTL8111H/RTL8111HS, proper PCB design is required. The following are some recommendations for better surge protection of line-to-ground mode defined in the IEC-61000-4-5 specification.

11.1. General Guidelines

- There should be more than 30 mils spacing between different differential pairs of MDI signals. In addition, MDI signal trace routing between the magnetics and the RJ-45 connector should have clearance constraint from other traces with a minimum of 100 mils spacing
- Keep 75ohm termination resistors and high voltage capability capacitors away from other component pads (min 50 mils)
- For 75ohm termination resistors we recommend to use 0603 or larger resistors, with a maximum overload voltage specification of at least 100V
- Trace routing from the magnetics RJ-45 jack side through 75ohm termination resistors and a high voltage capability capacitor to the Chassis GND should be as wide as possible to make sure the whole discharge path is wide enough
 - The trace width should be more than 40 mils
 - Use at least 3 solder-filled blind vias (diameter ≥ 30 mils; drill size ≥ 20 mils) or a solder-filled through hole (diameter ≥ 60 mils; drill size ≥ 35 mils) if a layer change is needed

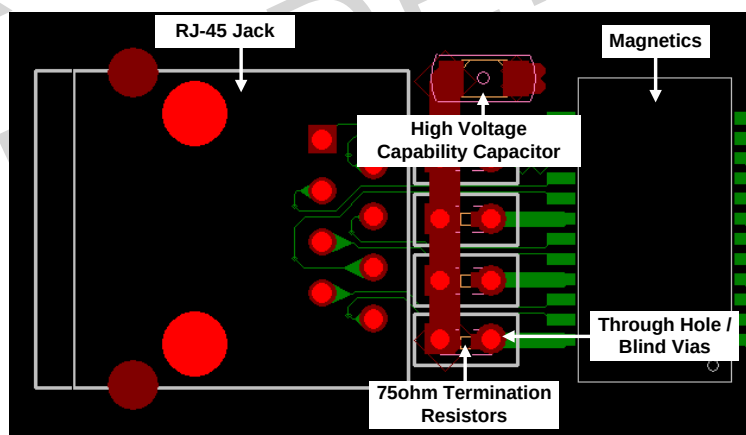


Figure 32. Trace Routing of the Magnetics RJ-45 Jack Side

- The power signal traces (power traces, ground traces) should be as short and wide as possible
- The plane area of the Chassis GND should be as large as possible. We recommend to have mounting screw holes on the board that connect the Chassis GND to the chassis
- The magnetics should be placed at least 1500 mils away from the RJ-45 jack

11.2. Special Layout Technique

A low-cost PCB design technique for surge protection of line-to-ground mode developed by Realtek is the spark gap (Patent Pending), which can be implemented as a part of the component pattern of a PCB. The spark gap can produce spark discharge in a short gap and provide overvoltage protection from a surge event such as that produced by lightning transients.

- We suggest two spark gap pads that have half circles with a radius of 20 mils, and with a gap between each of 8 mils. The pads must not be covered with solder mask (copper exposure) and the gap area must be open to the air. The spark gap design is shown in Figure 33

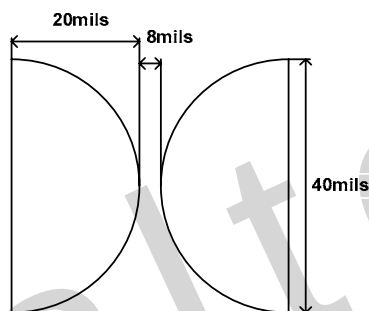


Figure 33. Spark Gap Design

- We recommend to place all spark gaps, 75ohm termination resistors, and a high voltage capability capacitor on the opposite side of the magnetics in the clear area, and keep these away from other component pads (minimum of 150 mils)
- The spark gap should be located between the source of the discharge path, e.g., the center tap of RJ-45 jack side of the magnetics, and the Chassis GND. The purpose is to generate a second discharge path and help to dissipate very high amplitude and fast rising surge voltage

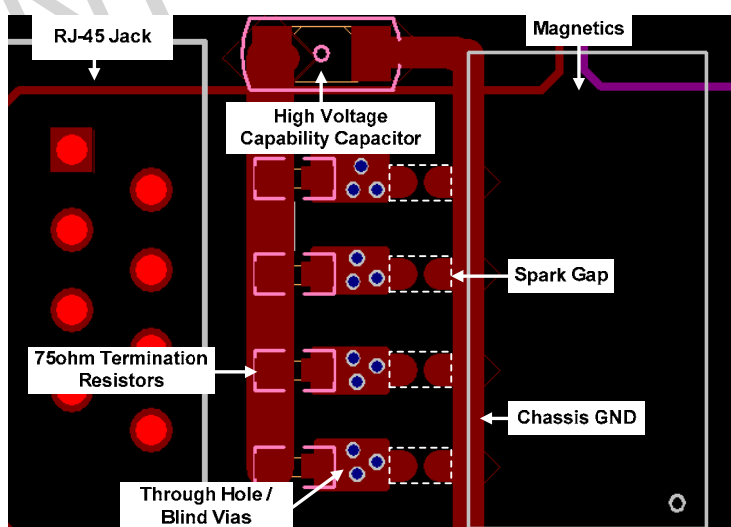


Figure 34. Spark Gap Layout

12. Special Notes

The analog GND pins must maintain a good ground return path. To do this, avoid using single-ended grounds, enlarge the analog GND plane, and try to keep the analog circuit return back to the real GND (from PCI) as short as possible. This is particularly important for 10/100/1000M Ethernet applications.

- If there is found to be a serious EMI issue, some de-coupling capacitors (0.01 μ F, 10 μ F) can be added between the system GND and power planes
- When using the oscillator as the clock source for 25MHz/48MHz, avoid connecting any capacitors to the clock circuitry
- To achieve proper skew rate requirements, the digital bus traces for BOOTROM should have lengths as equal as possible
- Keep a void area of at least 100 mils from the edge of each layer (e.g., power plane, GND plane, etc.) to the PCB edge in order to minimize fringe effect and lower EMI emissions

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